Listing of Claims

1. (Currently amended) A method of erasing an electrically erasable programmable read only memory cell that includes a source region, a drain region and control gauge electrode to which an erase signal is applied, the method comprising:

applying a source bias voltage to the source region;

applying a drain bias voltage to the drain region; and

applying a radio frequency/time domain based voltage signal to the control gate electrode of the cell as the erase signal.

2. (Original) A method as in claim 1, and wherein the frequency/time domain based voltage signal comprises a pulsed signal.

3. (Cancelled)

4. (New) A method as in claim 2, and wherein the amplitude of the pulsed signal is about twice the amplitude of a supply voltage signal provided to the cell.